UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,668	02/20/2002	Shrenik Deliwala	53168-500301D6	1405

7590 02/28/2003

Daniel H. Golub
1701 Market Street
Philadelphia, PA 19103

EXAMINER
CONNELLY CUSHWA, MICHELLE R

ART UNIT	PAPER NUMBER
2874	

DATE MAILED: 02/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/079,668	DELIWALA, SHRENIK	
	Examiner	Art Unit	
	Michelle R. Connelly-Cushwa	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-38* is/are pending in the application.

4a) Of the above claim(s) *13,14,21-27 and 33-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,15-20,28-32,37 and 38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *12-38* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *20 February 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5,8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Claims 13, 14, 21-27 and 33-36 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to non-elected inventions, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 9.

Information Disclosure Statement

The prior art documents submitted by applicant in the Information Disclosure Statements filed on February 20, 2002; April 15, 2002; and November 1, 2002 have all been considered and made of record (note the attached copies of form PTO-1449).

Drawings

This application has been filed with fifty-five (55) sheets of informal drawings, which are acceptable for examination purposes only.

The proposed drawing corrections filed on February 20, 2002 are approved. Corrected formal drawings are required in response to this Office action.

Specification

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12, 15-20, 28-32 and 37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 12; the claim recites the limitation "the light coupling portion" in line 8 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 20; the claim contains the limitation "thickness of less than 0.5μ" in line 2 of the claim. "μ" does not specify a unit for thickness. Examiner suggests changing "μ" to –μm—to overcome this rejection.

Regarding claims 15-20, 28-32 and 37; the claims inherently contain the deficiencies of any base or intervening claims from which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 12, 17, 20, 28, 30, 31, 32 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Weidel (US 4,966,430).

Regarding claims 12, 17, 20, 28 and 38; Figures 1-3 of Weidel disclose hybrid active electronic and optical circuits integrated within a SOI wafer, comprising:

- insulating silicon layers (4);
- waveguides (5) located within the silicon layers (4);
- active electronic circuits (3) positioned proximate waveguides (5);
- evanescent coupling regions at least partially located within silicon layers (4, 5) for optically coupling a light coupling portion to the waveguides (5) at a suitable angle;
- light deflectors (8) at least partially located in the silicon layers (4) and configured to deflect light impinging at the suitable incident angle to a suitable mode angle wherein light deflected by the light deflectors (8) enters the waveguides (5); and
- input and output couplers that couple light into and out of the waveguides (5);
- wherein the evanescent coupling regions are partially formed from air; and
- wherein the coupling region may have a thickness of less than 0.5 micrometers (see column 3, lines 13-44).

Regarding claim 30; in column 5, lines 16-27, Weidel discloses that the invention may comprise an optical multiplexer.

Regarding claims 31 and 32; in column 1, lines 17-30 and 55-40, Weidel discloses that the integrated circuit may include diodes and/or transistors.

Claims 12, 15, 18, 19, 28, 31, 32, 37 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Magel (US 5,502,779).

Regarding claims 12, 15, 18, 19, 28, 31, 32, 37 and 38; Figures 1a, 1b and 2a-2c of Magel disclose an integrated circuit comprising:

- a silicon substrate (12);
- an insulating layer (16);
- upper silicon layers (18, 20);
- waveguiding regions (18, 20);
- a transistor (optical device shown as 14, 27, 29);
- an active electronic circuit (the circuit including transistor; 14, 27, 29) proximate the waveguiding regions (18, 20, see Figure 2a)
- an evanescent coupling region located within the upper silicon layers, the evanescent coupling region optically coupling light (32a, 32b) at a suitable angle from a light coupling portion to a waveguiding region (18); and
- light deflectors (22, 24) located in the upper silicon layers and configured to deflect light (32b) impinging at the suitable incident angle to a suitable mode angle, wherein light deflected by the light deflector

(22) enters the waveguiding region (18) and light deflected by the light deflector (24) enters the waveguiding region (20);

- wherein the evanescent coupling region includes a substantially constant thickness gap portion;
- wherein the evanescent coupling region is formed from an optically clean polymer;
- wherein altering an electric voltage applied to the active electronic circuit affects a free carrier distribution in a region of the at least one optical device and thereby changes an effective mode index of the at least one optical device (see column 3, lines 3-64);
- wherein the light deflectors (22, 24) function as input/output couplers to couple light into and out of a waveguiding region (18), respectively, and out of and into a waveguiding region (20), respectively;
- wherein the optical device (transistor) is a p-n device (see column 3, lines 54-64); and
- wherein the circuit may include a p-i-n diode (see column 4, lines 54-58).

Claims 12, 15, 18, 19, 28-30, 37 and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Paniccia et al. (US 6,393,169 B1).

Regarding claims 12, 18, 19, 30 and 38; Paniccia et al. discloses a hybrid active electronic and optical circuit within an SOI wafer in Figure 8, the circuit comprising:

- an insulator layer (805, 809);

- a silicon layer (807);
- a waveguide located within the silicon layer (807) for receiving light (819);
- an active electronic circuit (811, 813, 815, 817) positioned proximate the waveguide, wherein a flow of light (819) through the waveguide can be altered depending on a property of the active electronic circuit;
- an evanescent coupling region (821, 825, 829) at least partially located within the upper silicon layer and formed from an optically clean polymer, wherein the evanescent coupling region optically couples the light coupling portion to the waveguide, and wherein light emitted from the light coupling portion can pass via the evanescent coupling region to the waveguide at a suitable angle;
- a light deflector (825) at least partially located in the silicon layer (807), the light deflector being configured to deflect light (819) impinging at a suitable mode angle wherein light deflected by the light deflector enters the waveguide;
- wherein altering an electric voltage (817) applied to the active electronic circuit affects a free carrier distribution in a region of at least one optical device, and thereby changes an effective mode index of the at least one optical device to form a modulator (see column 12, line 60, through column 17, line 28.)

Regarding claim 15; the evanescent coupling region includes a substantially constant thickness gap portion (821).

Regarding claim 28; the circuit includes input and output couplers (821, 823, 825, 827, 829, 831) that couple light into and out of the waveguide.

Regarding claim 29; the gratings (829, 831) disclosed by Paniccia et al. form a Fabry-Perot cavity.

Regarding claim 37; the circuit may include a p-n device (see Figure 9 and the corresponding description.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Paniccia et al. (US 6,393,169 B1).

Regarding claim 16; Paniccia et al. discloses all of the limitations of claim 16 as applied above, except for specifically stating that the evanescent coupling region is at least partially formed using an optically clear adhesive. In column 13, line 61, through column 14, line 22, Paniccia et al. discloses that the evanescent coupling region may be formed from material having an index of refraction approximately the same as the silicon layer or a material having a refractive index between that of the substrate and the silicon layer. Optically clear adhesives having refractive indices with the ranges

required by the invention of Paniccia et al. are well known and readily available in the art. One of ordinary skill in the art would have found it an obvious design choice to form the evanescent coupling regions (821, 823) disclosed by Paniccia et al. by any well known readily available materials that have suitable refractive indices, including optically clear adhesives, since Paniccia et al. does not disclose that specific materials are to be used, optically clear adhesives are well known and commonly used to form coupling regions in the art, Applicant has not disclosed that the use of optically clear adhesive solves any stated problem or is for any particular purpose, and it appears that the invention would perform equally well with any well known and commonly used materials having the appropriate refractive indices as taught by Paniccia et al.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Masi (US 3,951,513) discloses a semiconductor light modulating optical waveguide that may be formed from silicon materials and includes a silicon wafer (12); an optical waveguiding layer (10); evanescent coupling regions (20, 26) for coupling light (18) in the waveguiding layer (10); and an electric circuit (14, 16, 28, 30) proximate the waveguiding layer (10).

Isobe et al. (US 4,932,743) discloses an optical waveguide device in Figure 11, comprising a silicon substrate (11), an insulating/buffer SiO_2 layer (18) formed on the substrate; a SiN optical waveguide layer (12) formed on the insulating/buffer layer (18); and an evanescent coupling region including a prism

(13) and a gap/opening (14a) of constant thickness for coupling light into the waveguide (12); wherein the gap/opening (14a) may be filled with air or a dielectric material having an appropriate refractive index, including an optically clear polymer or an optically clear adhesive (see column 7, lines 7-33) for coupling light into the waveguide layer.

Kataoka (US 5,444,567) discloses an electro-optic integrated circuit including prisms (1) or gratings (13) in the evanescent coupling regions that couples light (8) into a waveguide (see Figures 3 and 9).

Agahi et al. (US 5,559,912) discloses wavelength selective devices using SOI technology.

Brown (US 5,625,729) discloses a opto-electronic device for coupling into an SOI device (see Figure 8).

Katoh et al. (US 5,719,981) discloses an integrated circuit including an evanescent coupling region (11, 10) for coupling light (12) into a waveguiding portion (5) formed in an insulating layer (3, 4) on a silicon substrate (1a, see Figure 1).

Mehlhorn et al. (US 6,285,808 B1) discloses a circuit carrier with an optical layer and an optoelectronic component.

Lee et al. (US 6,316,281 B1) discloses a method for fabricating a hybrid optical integrated circuit employing SOI optical waveguides.

Strake (US 6,370,292 B1) discloses a printed circuit board and method for its manufacture, wherein the printed circuit board includes an evanescent

coupling region for coupling light into waveguides that are formed in a layered stack, and an electrical circuit in proximity to the waveguides.

Liu et al. ("High-modulation-depth and short-cavity-length silicon Fabry-Perot modulator with two grating Bragg reflectors") discloses a Fabry-Perot modulator formed on an SOI substrate.

Any inquiry concerning the merits of this communication should be directed to Examiner Michelle R. Connelly-Cushwa at telephone number (703) 305-5327. Any inquiry of a general or clerical nature (i.e. a request for a missing form or paper, etc.) should be directed to the Technology Center 2800 receptionist at telephone number (703) 308-0956 or to the technical support staff supervisor at telephone number (703) 308-3072.

Michelle R. Connelly-Cushwa
MRCC
Patent Examiner

February 20, 2003